Amendments to the Claims are reflected in the listing of the Claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-20. (canceled)

21. (currently amended) A wafer level chip scale package comprising;

a semiconductor die having a plurality of pads on a surface;

pillar conductors coupled to and extending vertically a first predetermined distance from said surface of said semiconductor die;

an etch resistant layer on free ends of said ~~vertical~~ pillar conductors;

an epoxy layer on said surface, said epoxy layer having an exposed surface a second predetermined distance from said surface of said semiconductor die, wherein said second predetermined distance is less than said first predetermined distance and wherein said epoxy layer partially covers lower portions of side surfaces of substantially all of said pillar conductors; and

reflowable material attached to said etch resistant layer and to at least portions of side surfaces not covered by said epoxy layer of substantially all of said pillar conductors.

22. (currently amended) A wafer level chip scale package in accordance with claim 21

wherein the pillar conductors comprise copper pillar conductors.

23. (currently amended) A wafer level chip scale package in accordance with claim 22 wherein each of the copper pillar conductors comprise a plurality of plated copper layers.

24. (original) A wafer level chip scale package in accordance with claim 21 wherein the etch resistant layer comprises a layer of gold.

25. (original) A wafer level chip scale package in accordance with claim 21 wherein the etch resistant layer comprises a layer of nickel with a layer of gold thereon.

26. (original) A wafer level chip scale package in accordance with claim 25 wherein the thickness of the layer of gold is less than the difference between the first predetermined distance and the second predetermined distance.

27. (canceled)

28. (original) A wafer level chip scale package in accordance with claim 21 wherein the reflowable material comprises solder.

29. (original) A wafer level chip scale package in accordance with claim 28 wherein the solder comprises eutectic solder.

30-58. (canceled)